Subject: Re: vector of bin indices using histogram?
Posted by Foldy Lajos on Wed, 18 Oct 2006 15:53:21 GMT
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> CPU latency. Eg. for Pentium 4, the latency is 7 clock cycles for FMUL, and
> 43 for FDIV (this is worst case, depends on the data, and assumes that the
> data is in the L1 cache). Decent compilers (including
> FL :-) replace division by float const by multiplication.
>
> regards,
> lajos
>

oops, I have to correct myself: FDIV latency is 23 clock cycles for float,
38 for double, and 43 for long double. Anyway, it is greater than 7.

regards,
lajos